EXPEDITED PROCEDURE - EXAMINING GROUP 2829

S/N 09/785,006

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Aaron M. Schoenfeld	Examiner: Evan T Pert
Serial No.:	09/785,006	Group Art Unit: 2829
Filed:	February 16, 2001	Docket: 303.259US3
Title:	GRINDING TECHNIQUE FOR INTEGRATED CIRCUITS	

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

Box AF
Commissioner for Patents
Washington, D.C. 20231

In response to the Final Office Action mailed April 25, 2002, please amend the application as follows:

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 39 and 41. The specific amendments to claims 39 and 41 are detailed in the following marked up claims.

39. (Twice Amended) The semiconductor die as recited in claim 35, wherein each of the planar perimeter surfaces have polished surfaces.

41. (Amended) A semiconductor die comprising:

a first planar surface;

a second planar surface opposite the first planar surface;

one or more perimeter edges [disposed] transverse to and extending between the first planar surface and the second planar surface; and

at least one perimeter edge having two or more offset planar surfaces, where the offset planar surfaces are substantially transverse to the first planar surface or the second planar surface; and